**THEORY OF OPERATION**

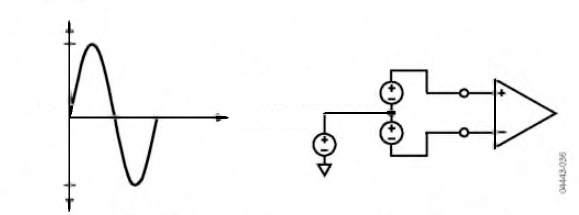
**ANTIALIASING FILTER**

This filter prevents aliasing, which is an artifact of all sampled systems. Input signals with frequency components higher than half the ADC sampling rate distort the sampled signal at a frequency below half the sampling rate. This happens with all ADCs, regardless of the architecture. The combination of the high sampling rate Z-A ADC used in the ADE7758 with the relatively low bandwidth of the energy meter allows a very simple lowpass filter (LPF) to be used as an antialiasing filter. A simple RC filter (single pole) with a corner frequency of 10 kHz produces an attenuation of approximately 40 dB at 833 kHz. This is usually sufficient to eliminate the effects of aliasing.

**ANALOG INPUTS**

The ADE7758 has six analog inputs divided into two channels: current and voltage. The current channel consists of three pairs of fully differential voltage inputs: IAP and IAN, IBP and IBN, and ICP and ICN. These fully differential voltage input pairs have a maximum differential signal of ±0.5 V. The current channel has a programmable gain amplifier (PGA) with possible gain selection of 1, 2, or 4. In addition to the PGA, the current channels also have a full-scale input range selection for the ADC. The ADC analog input range selection is also made using the gain register (see Figure 38). As mentioned previously, the maximum differential input voltage is ±0.5 V. However, by using Bit 3 and Bit 4 in the gain register, the maximum ADC input voltage can be set to ±0.5 V, ±0.25 V, or ±0.125 V on the current channels. This is achieved by adjusting the ADC reference (see the Reference Circuit section).

Figure 36 shows the maximum signal levels on the current channel inputs. The maximum common-mode signal is ±25 mV, as shown in Figure 37.



**V1 +** **V2**

**+500mV**

**VCM**

**-500m V**

**DIFFERENTIAL INPUT**

**V1 + V2 = 500mV MAX PEAK**

**COMMON-MODE**

**±25mV MAX**

**V1**

**V2**

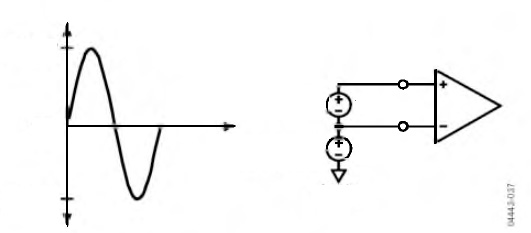
**IAP, IBP,   
OR ICP**

**IAN, IBN, OR ICN**

*Figure 36. Maximum Signal Levels, Current Channels, Gain = 1*

The voltage channel has three single-ended voltage inputs: VAP, VBP, and VCP. These single-ended voltage inputs have a maximum input voltage of ±0.5 V with respect to VN. Both the current and voltage channel have a PGA with possible gain selections of 1, 2, or 4. The same gain is applied to all the inputs of each channel.

Figure 37 shows the maximum signal levels on the voltage channel inputs. The maximum common-mode signal is ±25 mV, as shown in Figure 36.



**V2**

**+500mV**

**VCM**

**-500m V**

**SINGLE-ENDED INPUT**

**±500mV MAX PEAK**

**COMMON-MODE**

**±25mV MAX**

**V2**

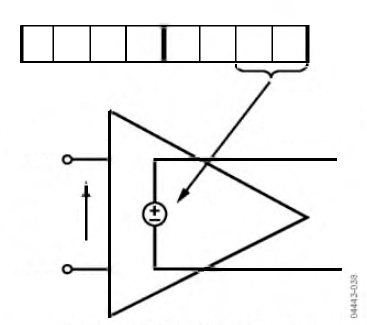
**Vcm**

**VAP, VBP, OR VCP**

**AGND**

*Figure 37. Maximum Signal Levels, Voltage Channels, Gain = 1*

The gain selections are made by writing to the gain register. Bit 0 to Bit 1 select the gain for the PGA in the fully differential current channel. The gain selection for the PGA in the singleended voltage channel is made via Bit 5 to Bit 6. Figure 38 shows how a gain selection for the current channel is made using the gain register.



**GAIN[7:0]**

**GAIN (K) SELECTION**

**IAP, IBP, ICP**

**VIN**

**K x VIN**

**IAN, IBN, ICN**

*Figure 38. PGA in Current Channel*

Figure 39 shows how the gain settings in PGA 1 (current channel) and PGA 2 (voltage channel) are selected by various bits in the gain register.

**GAIN REGISTER1**

**CURRENT AND VOLTAGE CHANNEL PGA CONTROL**

**ADDRESS: 0x23**

**PGA 1 GAIN SELECT**

**00 = х 1**

**01 = х 2**

**10 = х 4**

**RESERVED**

**CURRENT INPUT FULL-SCALE SELECT**

**00 = 0.5V**

**01 = 0.25V**

**10 = 0.125V**

**PGA 2 GAIN SELECT**

**00 = x 1**

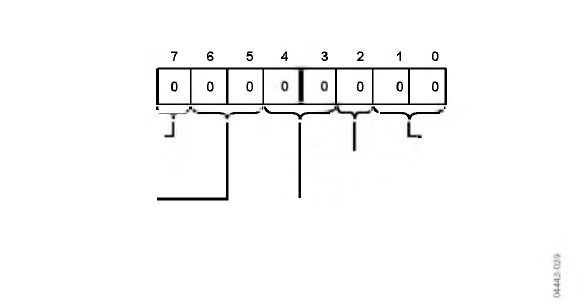
**01 = х 2**

**10 = х 4**

**INTEGRATOR ENABLE**

**0 = DISABLE**

**1 = ENABLE**



1REGISTER CONTENTS SHOW POWER-ON DEFAULTS

*Figure 39. Analog Gain Register*

Bit 7 of the gain register is used to enable the digital integrator in the current signal path. Setting this bit activates the digital integrator (see the DI/DT Current Sensor and Digital Integrator section).

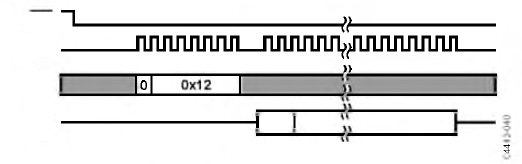
**CURRENT CHANNEL ADC**

Figure 41 shows the ADC and signal processing path for the input IA of the current channels (same for IB and IC). In waveform sampling mode, the ADC outputs are signed twos complement 24-bit data-words at a maximum of 26.0 kSPS (thousand samples per second). With the specified full-scale analog input signal of ±0.5 V, the ADC produces its maximum output code value (see Figure 41). This diagram shows a fullscale voltage signal being applied to the differential inputs IAP and IAN. The ADC output swings between 0xD7AE14 (-2,642,412) and 0x2851EC (+2,642,412).

***Current Channel Sampling***

The waveform samples of the current channel can be routed to the WFORM register at fixed sampling rates by setting the WAVSEL[2:0] bit in the WAVMODE register to 000 (binary) (see Table 20). The phase in which the samples are routed is set by setting the PHSEL[1:0] bits in the WAVMODE register. Energy calculation remains uninterrupted during waveform sampling.

When in waveform sample mode, one of four output sample rates can be chosen by using Bit 5 and Bit 6 of the WAVMODE register (DTRT[1:0]). The output sample rate can be 26.04 kSPS, 13.02 kSPS, 6.51 kSPS, or 3.25 kSPS. By setting the WFSM bit in the interrupt mask register to Logic 1, the interrupt request output IRQ goes active low when a sample is available. The timing is shown in Figure 40. The 24-bit waveform samples are transferred from the ADE7758 one byte (8-bits) at a time, with the most significant byte shifted out first.



**IRQ**

**SCLK**

**DIN**

**DOUT**

**READ FROM WAVEFORM**

**SGN**

**CURRENT CHANNEL DATA-24 BITS**

*Figure 40. Current Channel Waveform Sampling*



The interrupt request output IRQ stays low until the interrupt routine reads the reset status register (see the Interrupts section).

**GAIN[4:3]**

**2.42V, 1.21V, 0.6V**

**REFERENCE**

**GAIN[1:0]**

**x1, x2, x4**

**IAP**

**IAN**

**VIN**

**PGA1**

**ADC**

**HPF**

**GAIN[7]**

**DIGITAL**

**INTEGRATOR1**

**CURRENT RMS (IRMS) CALCULATION**

**WAVEFORM SAMPLE REGISTER**

**ACTIVE AND REACTIVE POWER CALCULATION**

**CHANNEL 1 (CURRENT WAVEFORM)**

**DATA RANGE AFTER INTEGRATOR**

**(50Hz AND AIGAIN[11:0] = 0x000)**

**50Hz**

**0x34D1B8**

**0x000000**

**0xCB2E48**

**CHANNEL 1 (CURRENT WAVEFORM)**

**DATA RANGE AFTER INTEGRATOR**

**(60Hz AND AIGAIN[11:0] = 0x000)**

**60Hz**

**0x2BE893**

**0x000000**

**0xD4176D**

**CHANNEL 1**

**(CURRENT WAVEFORM)**

**DATA RANGE**

**0x2851EC**

**0x000000**

**0xD7AE14**

**ADC OUTPUT WORD RANGE**

**ANALOG INPUT RANGE**

**VIN**

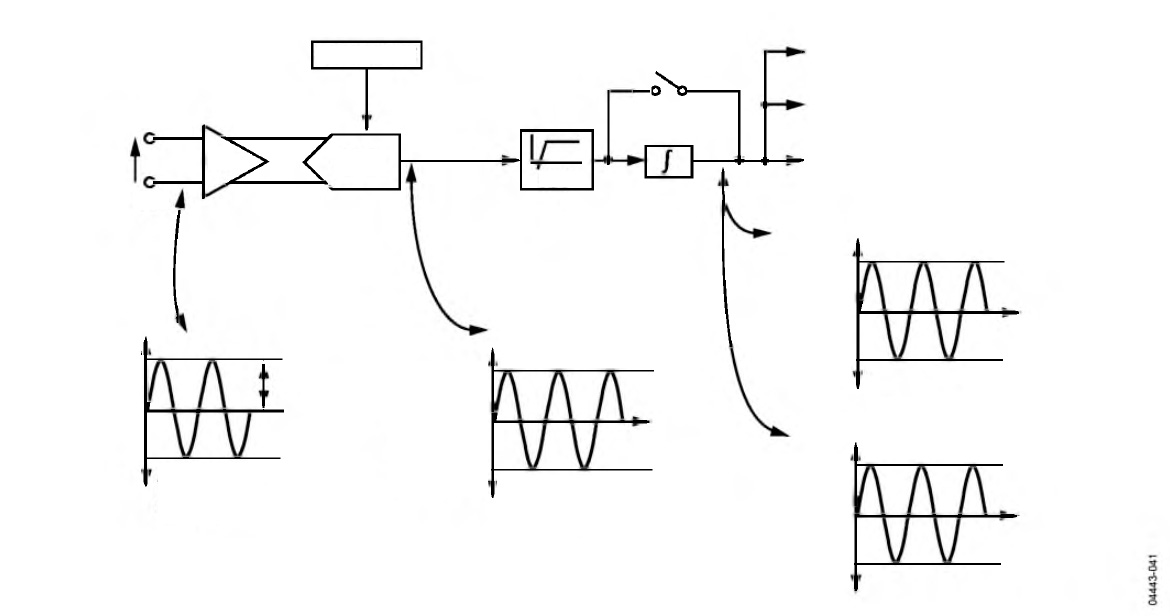
**0V**

**0.5V/GAIN**

**0.25V/GAIN**

**0.125V/GAIN**

**1WHEN DIGITAL INTEGRATOR IS ENABLED, FULL-SCALE OUTPUT DATA IS ATTENUATED DEPENDING ON THE SIGNAL FREQUENCY BECAUSE THE INTEGRATOR HAS A -20dB/DECADE FREQUENCY RESPONSE. WHEN DISABLED, THE OUTPUT WILL NOT BE FURTHER ATTENUATED.**



*Figure 41. Current Channel Signal Path*